AMENDMENTS TO THE CLAIMS

1. (Currently amended) A method for testing a memory device comprising:

placing said memory device in a test mode;

disconnecting ~~resetting~~ all match lines of said memory device from a priority encoder of said memory device;

confirming proper operation of a control line used to enable output from a match line under test;

connecting an ~~enabling~~ output from the match line under test to the priority encoder;

decoding an address of a selected memory storage location corresponding to said match line under test;

loading said selected memory storage location and a comparand register with a known data pattern;

performing a search operation, for the known data pattern in the comparand register, on said memory device;

outputting a result of said search operation;

comparing said result of said search operation with an expected result of said search operation, said expected result comprising an expected match indication on the match line under test;

confirming proper operation of said memory device if said result of said search operation is equal to said expected result of said search operation; and

indicating an error of said memory device if said result of said search operation is not equal to said expected result of said search operation.

2. (Original) The method according to claim 1, wherein said memory device is a content addressable memory (CAM) device.

3. (Original) The method according to claim 1, further comprising:

resetting output from said match line under test; and

enabling output from said memory storage location under test.

4. (Original) The method according to claim 1, wherein said resetting and said decoding acts occur on the rising edge of a clock signal.

5. (Original) The method according to claim 1, wherein said loading acts occur on the rising edge of a clock signal.

6. (Original) The method according to claim 1, wherein there is a one-to-one correspondence between said match lines and said memory storage locations.

7. (Original) The method according to claim 1, wherein there is a one-to-many correspondence between each said match line and said memory storage locations.

8. (Currently amended) A method of testing a memory device that includes two or more sets of memory cells and, for each set of memory cells, a match line that provides a match signal when items of data stored in said set of memory cells match a data item stored in a comparand register, the method comprising:

confirming proper operation of a control line used to enable output from said match line of a set of memory cells being tested;

connecting ~~enabling~~ said match line of the set of memory cells being tested to a priority encoder of the memory device;

disconnecting ~~and disabling~~ match lines of other sets of memory cells from the priority encoder;

storing items of data matching the data item stored in the comparand register in the set of memory cells being tested; and

receiving an output signal from said match line and determining whether said output signal indicates that said set of memory cells being tested has items of stored data that match the data item stored in a comparand register.

9. (Original) The method according to claim 8, in which said memory device is a content addressable memory (CAM) device.

10. (Previously presented) The method according to claim 8, in which each set of memory cells comprises a memory storage location associated with an address and the act of determining includes determining whether said output signals indicate addresses of said set of memory cells being tested.

Claims 11-16 (Canceled)

17. (Currently amended) A memory circuit comprising:

a set of memory cells that store items of data;

comparison circuitry that determines whether items of data stored in said set of memory cells match a data item stored in a comparand register and provides a match signal when said stored items of data match the data item stored in the comparand register; and

enabling circuitry that connects ~~enables~~ a match line to a priority encoder to provide said match signal as an output when said set of memory cells is being tested, said enabling circuitry ~~enabling~~ connecting the match line after disconnecting all match lines of the memory circuit and confirming proper operation of a control line.

18. (Canceled)

19. (Currently amended) The memory circuit according to claim 17, in which said set of memory cells stores said item of data, said memory circuit further comprising a word line that selects said set of memory cells, said enabling circuitry ~~enabling~~ connecting said match line in response to a signal on said word line.

20. (Currently amended) A memory device comprising:

two or more sets of memory cells, each set of memory cells storing an item of data;

for each set of memory cells, comparison circuitry that determines whether items of data stored in said set of memory cells match a data item stored in a comparand register and provides a match signal when said stored items of data match the data item stored in the comparand register;

for each set of memory cells, enabling circuitry that connects ~~enables~~ a match line to a priority encoder of the memory device to provide said match signal as an output when said set of memory cells is being tested;

for each set of memory cells, a word line that selects said set of memory cells, said enabling circuitry connecting ~~enabling~~ said match line in response to a signal on said word line, said enabling circuitry connecting ~~enabling~~ the match line after disconnecting all match lines of the memory circuit and confirming proper operation of a control line used to generate the signal on the word line; and

control circuitry that resets said enabling circuitry of all said sets of memory cells prior to testing so that none of said match lines are ~~enabled~~ to the priority encoder.

21. (Original) The memory device according to claim 20, in which said memory device is a content addressable memory (CAM) device.

22. (Previously presented) The memory device according to claim 20, in which each set of memory cells comprises a memory storage location associated with an address; the control circuitry determining whether said output signals indicate an address of said set of memory cells being tested.

Claims 23-32 (Canceled)

33. (Currently amended) An integrated circuit comprising:

two or more sets of memory cells, each set of memory cells storing an item of data;

for each set of memory cells, comparison circuitry that determines whether items of data stored in said set of memory cells match a data item stored in a comparand register and provides a match signal when said stored items of data match the data item stored in the comparand register;

for each set of memory cells, enabling circuitry that ~~enables~~ connects a single match line to a priority encoder to provide said match signal as an output when said set of memory cells is being tested;

for each set of memory cells, a word line that selects said set of memory cells, said enabling circuitry connecting ~~enabling~~ said single match line in response to a signal on said word line; and

control circuitry that resets said enabling circuitry of all said sets of memory cells prior to testing so that none of said match lines are connected to the priority encoder ~~enabled~~.

34. (Original) The integrated circuit according to claim 33, in which said memory device is a content addressable memory (CAM) device.

35. (Previously presented) The integrated circuit according to claim 33, in which each set of memory cells comprises a memory storage location associated with an address and the control circuitry determines whether said output signals indicate an address of said set of memory cells being tested.

Claims 36-38 (Canceled)

39. (Currently amended) A router comprising:

a memory device that comprises:

two or more sets of memory cells, each set of memory cells storing an item of data;

for each set of memory cells, comparison circuitry that determines whether items of data stored in said set of memory cells match a data item stored in a comparand register and provides a match signal when said stored items of data match the data item stored in the comparand register;

for each set of memory cells, enabling circuitry that connects ~~enables~~ a single match line to a priority encoder to provide said match signal as an output when said set of memory cells is being tested;

for each set of memory cells, a word line that selects said set of memory cells, said enabling circuitry ~~enabling~~ connecting said single match line in response to a signal on said word line; and

control circuitry that resets said enabling circuitry of all said sets of memory cells prior to testing so that none of said match lines are connected to the priority encoder ~~enabled~~.

40. (Currently amended) The router according to claim [[36]] 39, in which said memory device is a content addressable memory (CAM) device.

41. (Currently amended) The router according to claim [[36]] 39, in which each set of memory cells comprises a memory storage location associated with an address and the control circuitry determines whether said output signals indicate an address of said set of memory cells being tested.

42. (Currently amended) A system comprising:

a processor;

a content addressable memory (CAM) device coupled to said processor via a bus, said CAM device comprising an apparatus for testing a match line of said CAM device, said apparatus further comprising:

a memory storage location corresponding to a match line under test, said match line under test further having a corresponding word line;

a comparator coupled to at least one search line per CAM memory cell of said memory storage location; and

a circuit coupled to said match line under test corresponding to said word line, and a test mode match line reset signal, wherein said circuit performs the following functions:

placing said memory device in a test mode;

disconnecting ~~resetting~~ all match lines of said memory device from a priority encoder of said memory device;

confirming proper operation of a control line used to enable output from said match line under test;

connecting ~~enabling~~ said match line under test to the priority encoder;

decoding an address of a selected memory storage location corresponding to said match line under test;

loading said selected memory storage location with a known data pattern;

loading a comparand register with said known data pattern;

performing a search operation, for the known data pattern in the comparand register, on said memory device; and

outputting a result of said search operation;

comparing said result of said search operation with an expected result of said search operation, said expected result comprising an expected match indication on the match line under test;

confirming proper operation of said memory device if said result of said search operation is equal to said expected result of said search operation; and

indicating an error of said memory device if said result of said search operation is not equal to said expected result of said search operation.